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LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

ABSTRACT

A method and structure for forming an emitter in a vertical bipolar transistor includes providing a substrate having a collector layer and a base layer over the collector layer, forming a patterning mask over the collector layer,, and filling openings in the mask with emitter material in a damascene process. The CMOS/vertical bipolar structure has the collector, base regions, and emitter regions vertically disposed on one another, the collector region having a peak dopant concentration adjacent the inter-substrate isolation oxide.